AMENDMENTS TO CLAIMS

1. (Currently Amended) A method for executing a read request over a PCI bus by transferring data from a time-variant main memory of a first device to a second device, comprising the steps of:

obtaining an access request from a queue;

transferring, by a first DMA transfer, data from said time-variant main memory to a time-invariant second memory on said first device; and

transferring, by a second DMA transfer, said data from said time-invariant second memory to said second device.

2. (Canceled)

3. (Canceled)

4. (Original) The method of claim 1, wherein said second DMA transfer is initiated and said access request is selected by a finite state machine, which is associated with said queue.

5. (Currently Amended) The method of claim 1, wherein said second DMA transfer is initiated after said data transfer to said time-invariant second memory is terminated.

6. (Original) The method of claim 1, wherein said read request is a master read request hidden as a master write access of said first device.

7. (Original) The method of claim 6, wherein said master read request is directed to a target command queue of a finite state machine.

8. (Currently Amended) The method of claim 1, wherein said second device and said time-variant main memory are decoupled.

9. (Original) The method of claim 1, wherein data polling is avoided by transforming master read cycles of said second device to master write cycles of said first device.

10. (Currently Amended) A method for executing a write request over a PCI bus by transferring requested data from a second device to a time-variant main memory of a first device, comprising the steps of:

writing an access request to a queue;

transferring, by a first DMA transfer, data from said second device to a time-invariant second memory on said first device; and

transferring, by a second DMA transfer, said data from said time-invariant second memory to said time-variant main memory of said first device.

11. (Canceled)

12. (Currently Amended) The method of claim 10 ~~11~~, wherein said time-variant access behavior of said time-variant main memory is taken into consideration for said second DMA transfer.

13. (Canceled)

14. (Original) The method of claim 10, wherein said first DMA transfer is initiated by said second device.

15. (Original) The method of claim 10, wherein said second DMA transfer is initiated and said access request is selected by a finite state machine, which is associated with said queue.

16. (Currently Amended) The method of claim 10, wherein said second DMA transfer is initiated after said data transfer to said time-invariant second memory is terminated.

17. (Currently Amended) The method of claim 10, wherein said second device and said time-variant main memory are decoupled.

18. (Currently Amended) An apparatus for executing a read request over a PCI bus, comprising:

a queue for storing a read access request;

a time-variant main memory for storing data to be transferred;

a time-invariant buffer memory for buffer storage of said data, whereby data transfer to said time-invariant buffer memory is accomplished by a first DMA transfer;

a device located on the PCI bus for receiving said data, whereby data transfer from said time-invariant buffer memory to said device is accomplished by a second DMA transfer; and

a finite state machine associated with said queue for selecting an access request.

19. (Canceled)

20. (Canceled)

21. (Currently Amended) The apparatus of claim 18, wherein said time-variant main memory and said time-invariant buffer memory are located on a PCI card.

22. (Original) The apparatus of claim 18, wherein said finite state machine is adapted to initiate said second DMA transfer.

23. (Currently Amended) The apparatus of claim 18, wherein said second DMA transfer is initiated after said data transfer to said time-invariant buffer memory is terminated.

24. (Currently Amended) The apparatus of claim 18, wherein said device and said time-variant main memory are decoupled.

25. (Original) The apparatus of claim 21, wherein data polling is avoided by transforming master read cycles of said device to master write cycles of said PCI card.

26. (Currently Amended) An apparatus for executing a write request over a PCI bus, comprising:

a queue for storing a write access request;

a device located on a PCI bus for storing data to be transferred;

a time-variant main memory for receiving said data;

a time-invariant buffer memory for buffer storage of said data, whereby data transfer to said time-invariant buffer memory is accomplished by a first DMA transfer and data transfer from said time-invariant buffer memory to said time-variant main memory is accomplished by a second DMA transfer; and

a finite state machine associated with said queue for selecting an access request.

27. (Canceled)

28. (Currently Amended) The apparatus of claim 26 ~~27~~, wherein said time-variant access behavior of said main memory is taken into consideration for said second DMA transfer.

29. (Canceled)

30. (Currently Amended) The apparatus of claim 26, wherein said time-variant main memory and said time-invariant buffer memory are located on a PCI card.

31. (Original) The apparatus of claim 26, wherein said first DMA transfer is initiated by said devic .

32. (Original) The apparatus of claim 26, wherein said finite state machine is adapted to initiate said second DMA transfer.

33. (Currently Amended) The apparatus of claim 26, wherein said second DMA transfer is initiated after said data transfer to said time-invariant buffer memory is terminated.

34. (Currently Amended) The apparatus of claim 26, wherein said device and said time-variant main memory are decoupled.